

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
APPLICATION FOR UNITED STATES LETTERS PATENT

Title:

**METHOD OF FORMING TUNNEL OXIDE FILM  
IN SEMICONDUCTOR DEVICE**

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# METHOD OF FORMING TUNNEL OXIDE FILM IN SEMICONDUCTOR DEVICE

## BACKGROUND

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### 1. Field of the Invention

[0001] The present invention relates to a method of forming a tunnel oxide film in a semiconductor device and, more particularly, to a method of forming a tunnel oxide film in a semiconductor device capable of preventing degradation of film quality caused by absorbed carbon components and a rough surface on a semiconductor substrate.

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### 2. Discussion of Related Art

[0002] Figs. 1A to 1D are cross-sectional views for explaining a conventional method of forming a tunnel oxide film in a semiconductor device.

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[0003] Referring to Fig. 1A, in order to form a gate oxide film for a high voltage transistor, a first oxide film 2 having a thickness of 350 Å is formed on a semiconductor substrate 1 which has undergone predetermined processes.

20 [0004] Referring to Fig. 1B, a photo resist film 3 is formed on the first oxide film 2. Then, the photo resist film 3 is patterned to expose the first oxide film 2 formed on portions in which memory cells and low voltage transistors are to be formed.

**[0005]** Referring to Fig. 1C, the exposed portions on the first oxide film 2 are removed after the patterned photo resist film 3 is consolidated by a Descum process. In this case, the first oxide film 2 is removed by using a 300:1 BOE (Buffered Oxide Etchant) for a period of 2,280 seconds, and then  
5 the photo resist film 3 is removed by using H<sub>2</sub>SO<sub>4</sub> solution. Subsequently, a cleaning process is performed by using an SC-1 solution.

**[0006]** Referring to Fig. 1D, a second oxide film 4 having a thickness of 80 Å is formed on a whole top surface. In this case, a thick gate oxide film including the first oxide film 2 and the second oxide film 4 is formed in a high  
10 voltage transistor area, whereas a tunnel oxide film including the second oxide film 4 is formed in a memory cell area and a low voltage transistor area.

**[0007]** According to the conventional method, during the removal of the first oxide film 2 in a memory cell area and a low voltage transistor area by using a BOE, an over-etching of 30% occurs so that surface roughness of the  
15 semiconductor substrate 1 is increased and carbon components included in the photo resist film are absorbed on the surface of the semiconductor substrate 1 when the photo resist film 3 is removed by using H<sub>2</sub>SO<sub>4</sub> solution. The absorbed carbon components are seldom removed even by a subsequent cleaning process using an SC-1 solution or a preliminary cleaning process  
20 using a 50:1 HF solution before the tunnel oxide film is formed. As a result, the remaining carbon components bring about silicon dangling bonds. This makes film quality be degraded when a tunnel oxide film is formed under the state that the carbon components exist, whereby the resulted device may have a bad electrical property.

**[0008]** Figs. 2 and 3 are graphs showing the results of a constant current stress test (CCST) for a flash memory device according to the conventional method. The results show that uniformity of distribution is bad and a proportion of defect is also high. Particularly, most of initial defects are distributed in the edge portion of a wafer.

### SUMMARY OF THE INVENTION

**[0009]** Accordingly, the present invention is directed to provide a method of forming a tunnel oxide film in a semiconductor device in which a predetermined thickness of the oxide film is not removed during a process of removing the oxide film in a memory cell area and a low voltage transistor area after a gate oxide film for a high voltage transistor is formed, thereby preventing increase of surface toughness on a substrate and contamination caused by absorbed carbon components generated when the oxide films and the photo resist film are removed.

**[0010]** One aspect of the present invention is to provide a method of forming a tunnel oxide film in a semiconductor device, comprising the steps of: (a) forming a first oxide film on a semiconductor substrate, and then forming a photo resist pattern exposing the first oxide film in a memory cell area and a low voltage transistor area; (b) removing a predetermined thickness of the exposed first oxide film and the photo resist pattern sequentially; and (c) removing the remaining first oxide film completely and then forming a second oxide film on a whole surface.

**[0011]** In the aforementioned of a method of forming a tunnel oxide film in a semiconductor device according to another embodiment of the present invention, the first oxide film is a pure oxide film grown at a temperature of 750 °C to 850 °C to have a thickness of 350 Å to 600 Å.

5 **[0012]** In the aforementioned of a method of forming a tunnel oxide film in a semiconductor device according to another embodiment of the present invention, the step (b) further comprises steps of: removing a predetermined thickness of the first oxide film by using a 300:1 BOE for a period of 1,730 to 1,735 seconds; removing the photo resist pattern by using a  
10 H<sub>2</sub>SO<sub>4</sub> solution; and performing a cleaning process using an SC-1 solution to remove pollutants such as organic components or particles.

**[0013]** In the aforementioned of a method of forming a tunnel oxide film in a semiconductor device according to another embodiment of the present invention, a thickness of the first oxide film remaining after the step  
15 (b) is in the range of 17 Å to 23 Å, and the first oxide film is preferably removed by a cleaning process using a 50:1 HF solution in the step (c).

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0014]** The aforementioned aspects and other features of the present  
20 invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

**[0015]** Figs. 1A to 1D are cross-sectional views for explaining a conventional method of forming a tunnel oxide film in a semiconductor device;

**[0016]** Figs. 2 and 3 are graphs showing the results of a constant current stress test for a flash memory device according to a conventional method;

**[0017]** Figs. 4A to 4D are cross-sectional views for explaining a method of forming a tunnel oxide film in a semiconductor device according to the  
5 present invention;

**[0018]** Fig. 5 is a graph showing the result of a constant current stress test for a flash memory device according to the present invention; and

**[0019]** Fig. 6 is a plan view showing distribution of dies on a wafer together with the results of the constant current stress test.

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#### DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

**[0020]** The present invention will be described in detail by way of the preferred embodiment with reference to the accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

15 **[0021]** Figs. 4A to 4D are cross-sectional views for explaining a method of forming a tunnel oxide film in a semiconductor device according to the present invention.

**[0022]** Referring to Fig. 4A, in order to form a gate oxide film for a high voltage transistor, a first oxide film 12 having a thickness of 350 Å to  
20 600 Å is formed on a semiconductor substrate 11 which has undergone predetermined processes. The first oxide film 12 is made of a pure oxide grown at a temperature of 750°C to 850°C.

**[0023]** Referring to Fig. 4B, a photo resist pattern 13 is formed on the first oxide film 12 and then patterned to expose the first oxide film 12 in the areas that a memory cell and a low voltage transistor are to be formed.

**[0024]** Referring to Fig. 4C, a Discum process is performed at a  
5 temperature of 80°C to 140°C for a period of 10 minutes or less to consolidate the patterned photo resist film 13. Then, a predetermined thickness of the first oxide film 12 in each exposed portion is removed. Subsequently, a part of the first oxide film 12 is removed by a 300:1 BOE for a period of 1,730 to 1,735 seconds, the photo resist film 13 is removed by a H<sub>2</sub>SO<sub>4</sub> solution, and then a  
10 cleaning process is performed by an SC-1 solution so that pollutants such as organic components and particles are completely removed. In this case, the organic pollutants may be removed in such a way that a Caro's acid is formed by the reaction of H<sub>2</sub>SO<sub>4</sub>/H<sub>2</sub>O<sub>2</sub> at a high temperature of 80°C to 100°C, and then a dehydration and an oxidation are performed. The aforementioned  
15 processes including the process of removing the first oxide film 12, the process of removing the photo resist film 13, and the cleaning process are performed sequentially.

**[0025]** Referring to Fig. 4D, the remaining first oxide film 12 is completely removed by a pre-cleaning process FN40" using a 50:1 HF  
20 solution, and then the second oxide film 14 having a thickness of 80 Å is formed on a whole top surface. As a result, a thick gate oxide film including the first oxide film 12 and the second oxide film 14 is formed in a high voltage transistor area, and a tunnel oxide film including the second oxide film 14 is formed in a memory cell area and a low voltage transistor area.

**[0026]** The aforementioned second oxide film 14 is formed by an oxidation process using  $H_2/O_2/N_2$  gas and a heat treatment using  $N_2$  gas and has a thickness of  $80\text{ \AA}$  in a high voltage transistor area or  $350\text{ \AA}$  in a memory cell area and a low voltage transistor area. Meanwhile, a predetermined  
5 thickness of the first oxide film 12 in a high voltage transistor area may be removed during the aforementioned pre-cleaning process.

**[0027]** According to the present invention, as shown in Fig. 4C, a predetermined thickness, e.g., in the range of  $17\text{ \AA}$  to  $23\text{ \AA}$ , of the first oxide film 12 on the semiconductor substrate 11 is not removed during the process  
10 of removing the first oxide film 12 and the photo resist film 13. For this reason, it is possible to minimize increase of the surface roughness and damages on the semiconductor substrate 11 caused by the BOE and prevent contamination caused by the remaining carbon components included in the photo resist film 13. In addition, it is possible to improve carrier mobility and breakdown  
15 characteristic of the tunnel oxide film because the second oxide film 14 is formed immediately after the remaining first oxide film 12 is completely removed.

**[0028]** Fig. 5 is a graph showing the result of a current stress test characteristic for a flash memory device according to the present invention,  
20 where it is possible to recognize that the uniformity of the current stress test characteristic is improved as a whole to show an excellent characteristic and a proportion of initial defect is also decreased. In addition, as shown in Fig. 6, it is possible to recognize that there are only three defective dies on the edge portion of a wafer.



**[0029]** As described above, according to the present invention, a predetermined thickness of the oxide film is not removed during a process of removing the oxide film in a memory cell area and a low voltage transistor area after a gate oxide film for a high voltage transistor is formed, thereby  
5 preventing increase of surface roughness on a substrate and contamination caused by absorbed carbon components which are generated when the oxide films and the photo resist film are removed. Therefore, it is possible to form a tunnel oxide film having an excellent film quality, thereby improving an electrical property of the resulted device.

10 **[0030]** Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.

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